What is claimed is:

1. A semiconductor device, comprising a laterally diffused field effect transistor including, over a semiconductor substrate, an element-forming area and a scribing area surrounding the element-forming area, the transistor including:

(a) a semiconductor layer of a first conductive type formed in the element-forming area over the semiconductor substrate,

(b) a gate insulating film formed over the semiconductor layer,

(c) a gate electrode formed over the gate insulating film,

(d) a source comprised of a first semiconductor region of a second conductive type being different from the first conductive type,

(e) a drain comprised of a second semiconductor region of the second conductive type having a first impurity concentration, and a third semiconductor region of the second conductive type having a higher second impurity concentration than the first impurity concentration and formed at a position farther from the gate electrode than the second semiconductor region,

(f) a forth semiconductor region of the first

conductive type where a channel region is formed,

(g) an electrode electrically connected to the source and formed over the rear surface of the semiconductor substrate, and

(h) a source electrode pad, for evaluation, formed in the element-forming area over the front surface of the semiconductor substrate and electrically connected to the semiconductor substrate.

2. The semiconductor device according to claim 1, wherein the source electrode pad for evaluation is not formed in the scribing area.

3. The semiconductor device according to claim 1, wherein the source electrode pad for evaluation and the semiconductor substrate are connected to each other through a fifth semiconductor region of the first conductive type formed in the semiconductor layer.

4. The semiconductor device according to claim 1, wherein a passivation film is formed over the semiconductor substrate and the thickness from the rear surface of the semiconductor substrate to the front surface of the passivation film covering the source electrode pad for evaluation is 200 μm or less.

5. The semiconductor device according to claim 1, further comprising a drain electrode pad formed over the front surface of the semiconductor substrate and electrically connected to the third semiconductor region, and a gate electrode pad electrically connected to the gate electrode.

6. A semiconductor device, comprising a laterally diffused field effect transistor which includes:

(a) a semiconductor layer of a first conductive type formed over a semiconductor substrate;

(b) a gate insulating film formed over the semiconductor layer;

(c) a gate electrode formed over the gate insulating film;

(d) a source comprised of a first semiconductor region of a second conductive type being different from the first conductive type;

(e) a drain comprised of a second semiconductor region of the second conductive type having a first impurity concentration, and a third semiconductor region of the second conductive type having a higher second impurity concentration than the first impurity concentration and formed at a position farther from the

gate electrode than the second semiconductor region;

(f) a forth semiconductor region of the first conductive type where a channel region is formed;

(g) a sixth semiconductor region of the first conductive type formed in the semiconductor layer and being a region for connecting electrically the first semiconductor region and the semiconductor substrate to each other; and

(h) a trench formed between the first semiconductor region and the sixth semiconductor region so as to extend from the front surface of the semiconductor layer toward the semiconductor substrate.

7. The semiconductor device according to claim 6, further comprising a source electrode pad for evaluation formed over the front surface of the semiconductor substrate and electrically connected to the semiconductor substrate.

8. The semiconductor device according to claim 6, further comprising a drain electrode pad formed over the front surface of the semiconductor substrate and electrically connected to the third semiconductor region, and a gate electrode pad electrically connected

to the gate electrode.

9. The semiconductor device according to claim 6, wherein the depth of the trench is 2 μm or more.

10. The semiconductor device according to claim 6, wherein an insulating film is embedded in the trench.

11. The semiconductor device according to claim 6, wherein an electrically conductive film is embedded in the trench.

12. The semiconductor device according to claim 6, wherein the trench is formed around the sixth semiconductor region.

13. The semiconductor device according to claim 6, wherein the trench restrains the sixth semiconductor region from spreading to the channel region.

14. A method of manufacturing a semiconductor device, comprising steps of:

forming a laterally diffused field effect transistor which includes:

(a) a semiconductor layer of a first

conductive type formed over a semiconductor substrate;

(b) a gate insulating film formed over the semiconductor layer;

(c) a gate electrode formed over the gate insulating film;

(d) a source electrically connected to the semiconductor substrate and comprised of a first semiconductor region of a second conductive type being different from the first conductive type;

(e) a drain comprised of a second semiconductor region of the second conductive type having a first impurity concentration, and a third semiconductor region of the second conductive type having a higher second impurity concentration than the first impurity concentration and formed at a position farther from the gate electrode than the second semiconductor region;

(f) a forth semiconductor region of the first conductive type where a channel region is formed;

(g) an electrode electrically connected to the source and formed over the rear surface of the semiconductor substrate; and

(h) a source electrode pad, for evaluation, formed over the front surface of the semiconductor substrate and electrically connected to the

semiconductor substrate;

adhering a reinforcing tape onto the rear surface of the semiconductor substrate; and

bringing a probe into contact with the source electrode pad for evaluation, thereby measuring the characteristic of the field effect transistor.

15. The method of manufacturing the semiconductor device according to claim 14, wherein before the reinforcing tape is adhered onto the rear surface of the semiconductor substrate, the rear surface of the semiconductor substrate is polished.

16. The method of manufacturing the semiconductor device according to claim 14, wherein the semiconductor substrate is diced in the state that the reinforcing tape is adhered on the rear surface of the semiconductor substrate.

17. The method of manufacturing the semiconductor device according to claim 14, wherein the semiconductor substrate is scribed in the state that the reinforcing tape is adhered on the rear surface of the semiconductor substrate.

18. A method of manufacturing a semiconductor device comprising a laterally diffused field effect transistor, comprising the steps of:

(a) forming a semiconductor layer of a first conductive type over a semiconductor substrate;

(b) making a trench in the semiconductor layer,

(c) introducing a first impurity into the semiconductor layer, thereby forming a sixth semiconductor region of the first conductive type, reaching the semiconductor substrate from the trench, in the semiconductor layer in the side opposite to a channel region;

(d) forming a gate insulating film over the semiconductor layer;

(e) forming a gate electrode over the gate insulating film;

(f) introducing a second impurity into the semiconductor layer, thereby forming a second semiconductor region, for a drain, which is of a second conductive type different from the first conductive type in such a state that an end of the second semiconductor region is consistent with one end of the gate electrode; and

(g) introducing a third impurity into the semiconductor layer, thereby forming a third

semiconductor region, for a drain, which is of the second conductive type at a position where one end of the third semiconductor region is apart from the one end of the gate electrode by the length of the first semiconductor region, and further forming a first semiconductor region, for a source, which is of the second conductive type in such a state that one end of the first semiconductor region is consistent with the other end of the gate electrode.

19. The method of manufacturing the semiconductor device according to claim 18, further comprising the step of embedding an insulating film in the trench after the step (b).

20. The method of manufacturing the semiconductor device according to claim 18, further comprising the step of embedding an insulating film or an electrical conductor in the trench after the step (c).